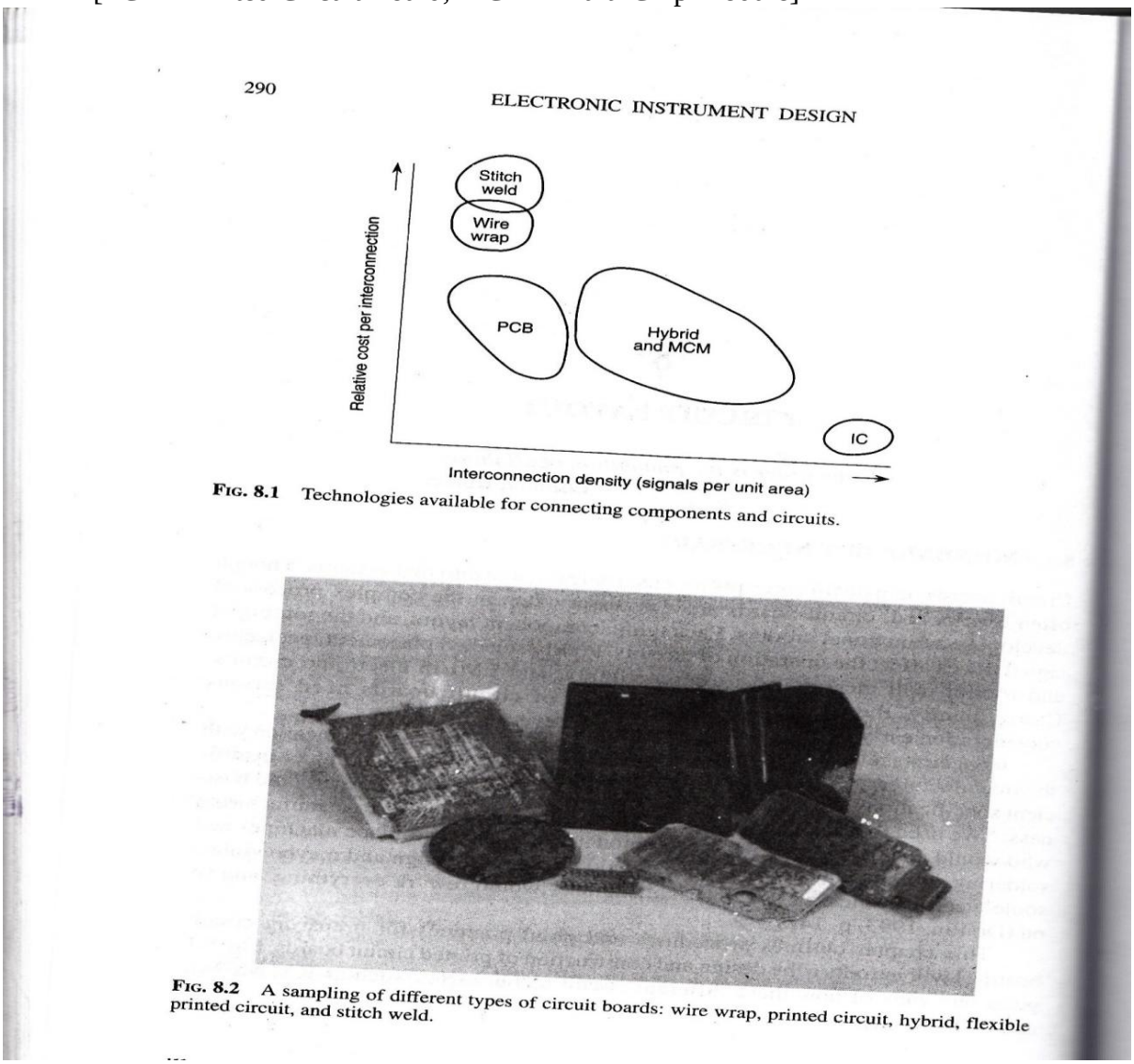
Chapter – 8
Circuit Layout

8.1 Circuits Boards and PCBs

- Technologies available for connecting components and circuits
- Circuit boards combine electronic components and connectors into a functional system through electrical connections and mechanical support.
- Stitch weld, Wire wrap, PCB, Chip on board, Hybrid and MCM
  [PCB= Printed Circuit Board, MCM= Multi Chip Module]



Wire-Wrap

- Easily change the connections, circuit modifications & corrections.
- Larger circuit boards, require extensive effort
- Less useful for production, suitable for prototype development
- Limited in operation to less than 5 or 10 MHz, above which the loop inductances in the wired connections distort signals.

Stitch Weld

- Connects components with point-to-point wiring on circuit boards much like wire wrap
- Stitch weld ports are shorter and the wire is welded to the pins, not wrapped, results lower loop inductance and much higher operation (100 MHz).
- Better vibration and shock resistance, more expensive, requires a special welding station.

PCB (Printed Circuit Board)

- Etched and plated connections
- Make automated placement and soldering of components possible
- Control impedances more effectively than wire-wrap
- Cost effective, manufacturing edge and reliability

Single Sided PCB

- Low frequency operation (< 25 KHz)
- Signal cross over wire jumpers are used

Double Sided PCB

- Signal traces on both sides of the circuit board and plated through vias.
- Can support higher frequency operation if laid out very carefully.

Multilayer PCB

- A stack of alternate layers of copper-clad laminate or core and prepreg.
- 20 to 30 conducting layers laminated together
- Control impedance much more tightly and are absolutely necessary for high frequency circuits
- Through-hole vias penetrate all layers and can connect signals on each layer.
- Buried vias connect traces on two sides of an internal layer
- Blind vias are exposed on one external layer and connect traces on the two sides of that layer.

MCM (Multi-Chip Module)

- Higher level of circuit density by bonding the base die of ICs onto a substrate
- Compact packing improves signal speeds and reduces load capacitance
- Expensive to fabricate

8.2 Component Placement

- Affects circuit operation, manufacturing edge, and the probability of design errors.
- General rules:
    1) Group high current circuit near the connector to isolate stray currents and near the edge of the PCB to remove heat.
    2) Group high frequency circuits near the connector to reduce path length, crosstalk and noise.
    3) Group low power and low frequency circuits away from high current and high frequency circuits
    4) Group analog circuits separately from digital circuits.

- Grouping components and circuits appropriately will reduce crosstalk and noise and will dissipate heat efficiently.

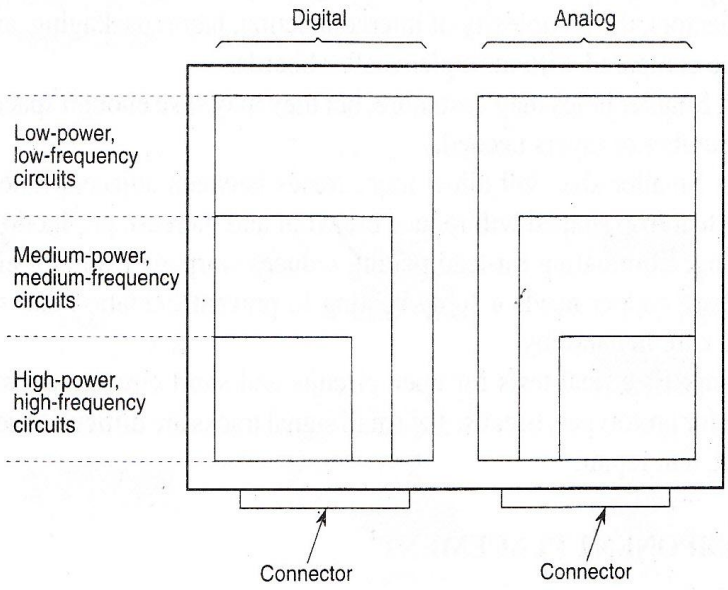


FIG. 8.7 Grouping of components. Arrange high-power and high-frequency circuits near the connector and away from the low-power circuits.

8.3 Routing Signal Traces

- Poor layout → false triggering of logic
- Due to formation of capacitive and inductive parasites with stubs, vias, IC pins, multiple loads and traces; setup and hold time violation and transmission delay.

8.3.1 Trace Density, Common Impedance, Distribution of signals and Return, Transmission Line Concerns, Trace Impedance and Matching, and Avoiding Crosstalk

Trace density

- Trade off between greater cost and difficulty in producing the denser circuit board.
- As you squeeze signal traces together on a board, you can space components closer and reduce the size of the circuit boards.
- Smaller boards, allowed by higher trace densities, provide flexibility in packaging your product, reduce the cost of material and may degrade signal integrity.

Common Impedance

- Minimize the number of circuits that share the same return path. Voltage drops (caused by current switching) on the ground line (return path) increase system noise.

- Common impedance paths cause components to reside at different ground potentials from one another.
- You can reduce the voltage drops, and hence the noise by lowering effective impedance
- Unbroken return plane is the best way.
- Choosing the right logic family and using decoupling capacitors will help by reducing the magnitude of current pulses.

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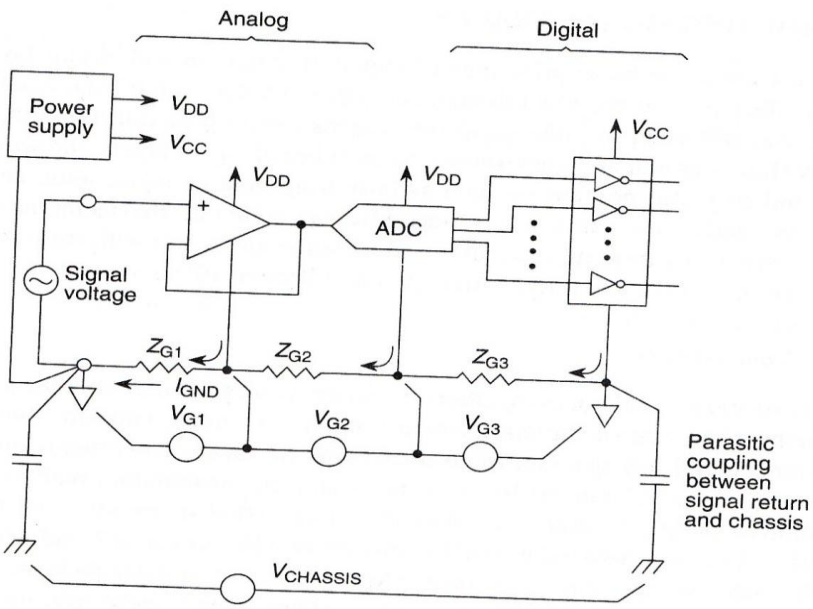


FIG. 8.8 Common impedance. Common-impedance paths cause components to reside at different ground potentials from one another. Larger common impedance will cause larger ground potentials (V_{G1}, V_{G2}, V_{G3}) and coupling to the chassis ($V_{CHASSIS}$); these will bias the signal voltage and introduce error.

Distribute signal and return

- Address the issues of return path early in design.
- Long return path can shift the ground potential excessively, decrease noise margins, and cause false switching.
- If the return is longer than signal, then the current has high inductance path that cause noise spikes in the ground system.
- Large loops of current have high inductance or impedance and radiated noise is often proportional to return path impedance and loop area.

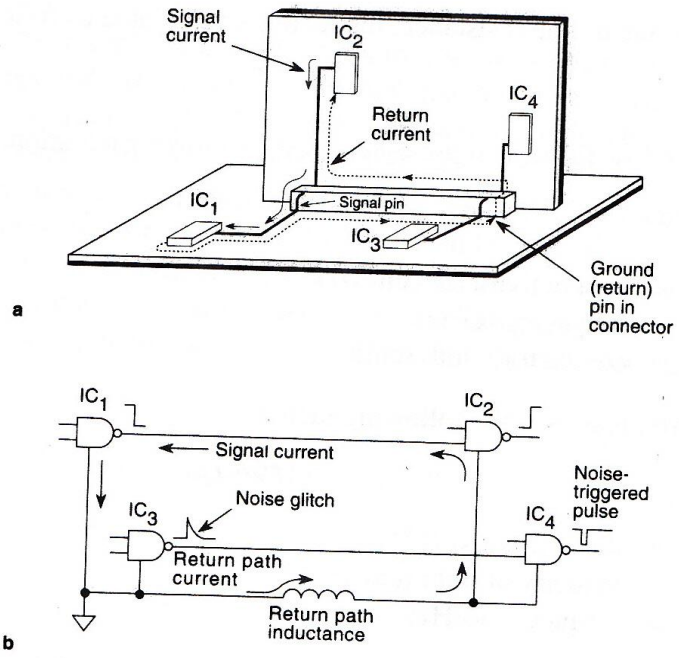


FIG. 8.9 Effect of ground pin placement. Poor placement of ground pins causes long return paths and large loop inductance. (a) The return current follows the path of lowest impedance in the ground under the signal trace, but it makes a long excursion to its connector pin. (b) Schematic representation of a long return path. The voltage across the inductance can cause the output of IC_3 to "glitch" high enough to trigger IC_4.

Transmission Line Concerns

- Signal conductors are never ideal transmission lines.
- Characteristic impedance: characteristic impedance Z_0 depends on frequency; higher frequencies attenuate more than lower frequencies.
- Dispersion: signals at different frequencies propagate at different speeds.
- Propagation delay: can corrupt circuit operation; depends on interconnection length and signal velocity
- Line resistance, skin effect and dielectric losses: degrade signals and introduce delay and error into circuit operation.

Trace impedance and impedance matching

- Impedance of signal conductors directly affects circuit operation.
- Low characteristic impedance (Z_0) radiates less and is less susceptible to interference than a circuit with higher impedance.
- Impedance mismatches lead to reflections that can both delay switching and trigger logic falsely.
  Reflection Coefficient = $(Z_L - Z_0) / (Z_L + Z_0)$
- Multiple loads have stubs, non-uniform impedance and mismatches that compromise noise margins.

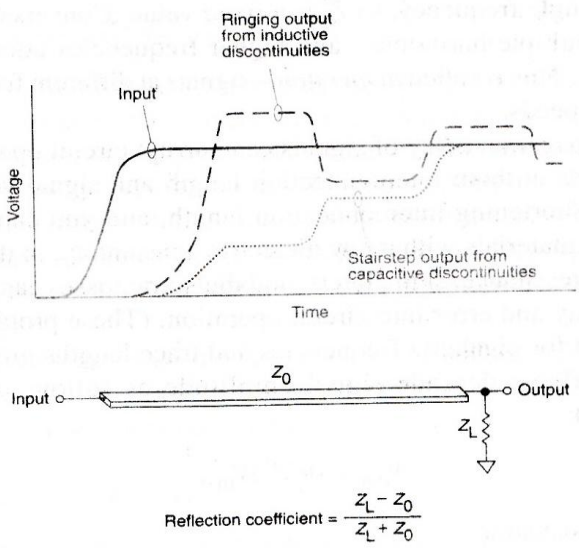


FIG. 8.10 Impedance mismatch and resulting degradation of signals along a printed circuit trace.

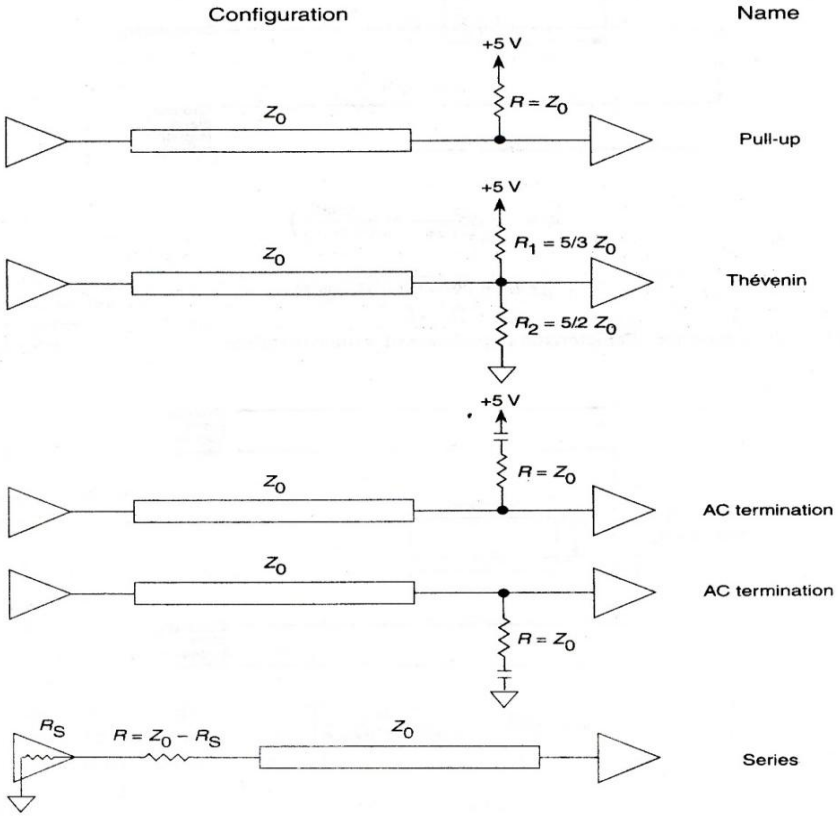
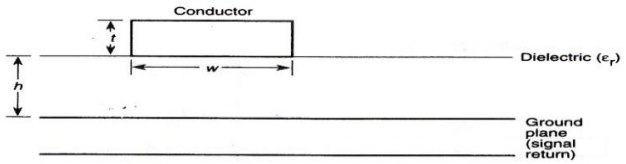


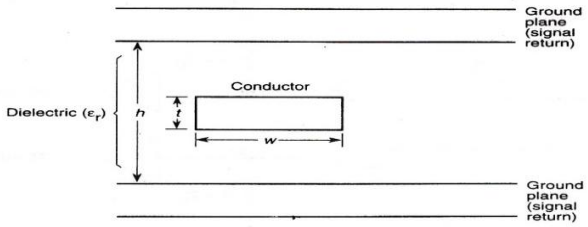
FIG. 8.11 A number of ways to terminate a signal trace.



$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

$$t_p = 3.339\sqrt{0.45\,\epsilon_r + 0.67} \text{ (ns/m)}$$

FIG. 8.12 Calculation for characteristic impedance of a microstripline.



$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \ln\left[\frac{4h}{0.67\,\pi\,(0.8w + t)}\right]$$

$$t_p = 3.339\sqrt{\epsilon_r} \text{ (ns/m)}$$

FIG. 8.13 Calculation for the characteristic impedance of a stripline.

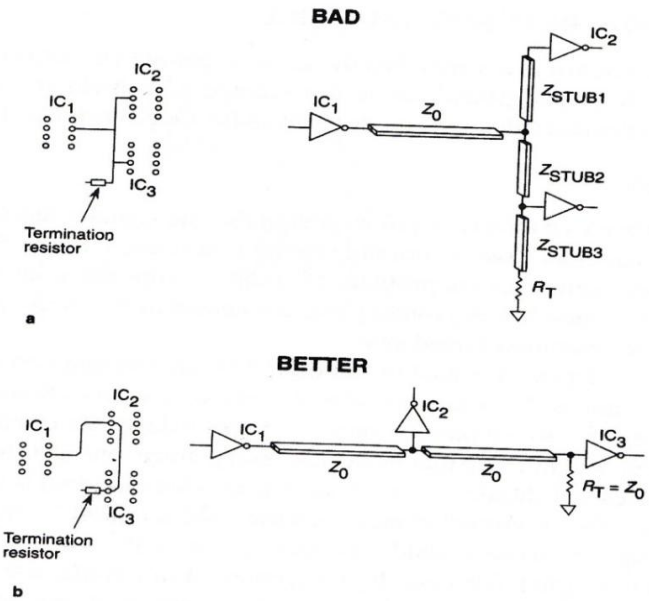


FIG. 8.14 Using a single serpentine trace to connect multiple inputs and eliminate stubs that cause reflections in the signal. (a) Poor layout degrades signal edges at the inputs to IC_2 and IC_3. (b) Using both a serpentine trace and a termination resistor near the last input eliminates stubs and preserves signal integrity.

Avoiding Crosstalk

- Simple guidelines when routing signal to a PCB:
  - Don't run parallel traces for long distances- particularly asynchronous signals.
  - Increase separation between conductors.
  - Shield clock lines with guard strips.
  - Reduce magnetic coupling by reducing the loop area of circuits.
  - Sandwich signal lines between return planes to reduce crosstalk.
  - Isolate the clock, chip select, chip enable, read and write lines

8.4 Ground, Returns and Shields

- Proper ground and return scheme will shield and suppress most EMI in electronics and reduce errors caused by noise.

- **Grounding**
  - Provides reference point for signal.
  - Signal reference should be a single point and is as close as possible to the power entry to the PCB.
  - A ground plane connected to the single-point reference will also reduce common impedance.
  - Be sure to separate the analog and digital circuits so that current pulses from digital circuits will not corrupt sensitive analog circuits. Use common ground plane or different planes and connect their ground leads to the single-point reference.

- **Distribute power and return carefully**
  - Address the issues of return path early in design.
  - Low impedance and minimum voltage drop within the power distribution of the PCB is desirable for optimum performance of circuits.
  - Reduce the inductive loop area between the powers and return traces.
  - Multilayer PCB → with power and return (or ground) planes.
  - Keep voltage drop less than 2% in the distribution of circuits.

- **Shielding**
  - A return plane is the most effective shield for any circuit.
  - Power and return planes provide circuit paths with the lowest impedance, which reduces radiation, noise and crosstalk.
  - Minimizing spacing between power and return will minimize impedance (radiation and susceptibility)

    $Z_0 = (120\pi/\sqrt{Er}) \cdot (h/d)$

    Where, h = separation of planes

    d = smaller dimension of two-dimensional plane

    Er = dielectric constant of substrate board relative to air

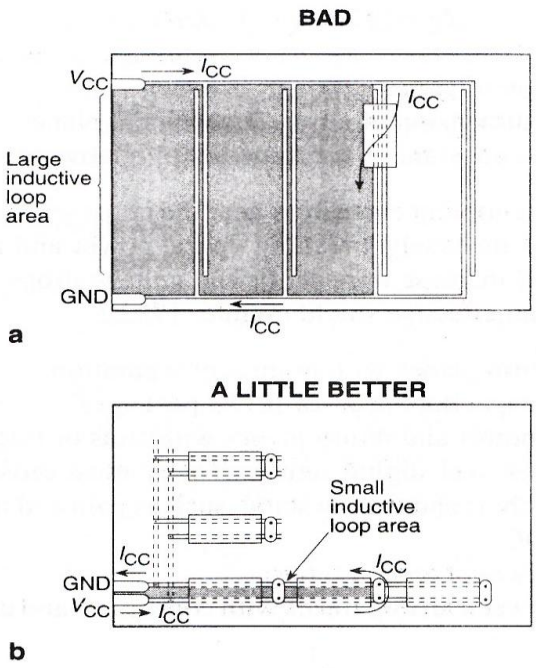


FIG. 8.15 Reducing inductive loop area. Orientation and location of the supply rails are important. (a) Interleaved combs arrangement can create large loops. (b) Running power and return together reduces the loop area. Johnson and Graham (1993) suggest a grid arrangement for the power and return rails to further reduce the loop area of signal currents, but return and power planes are by far the best solution.

- Guidelines for effective shield
  - Use power and return planes with minimum separation.
  - Place decoupling capacitors near (or in) IC packages.
  - Don't disrupt the power and return planes with slots or traces
  - Route digital traces over digital return.
  - Route analog traces over analog return.
  - Fill the regions between analog traces with copper foil and connect to ground.

6. Fill the regions bet...

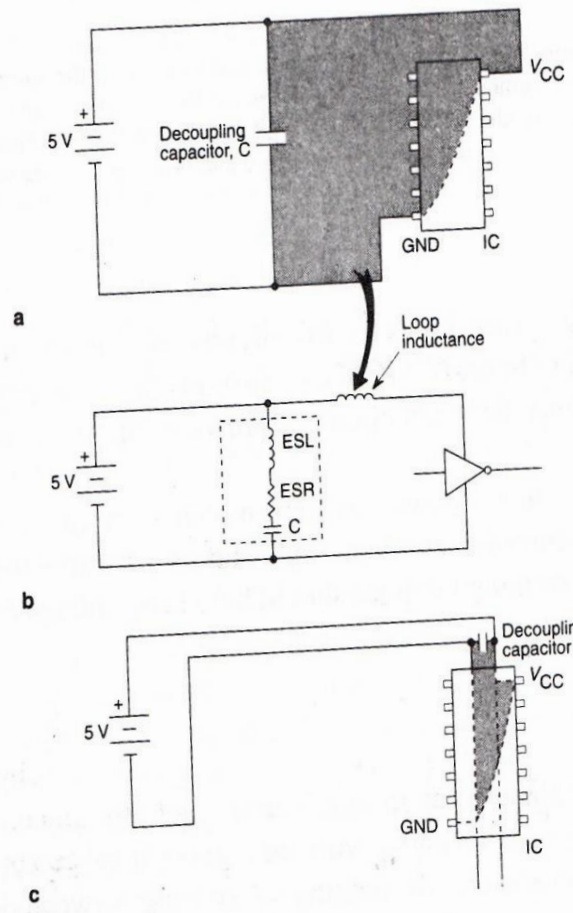


FIG. 8.16 Power supply decoupling. (a) Location of the decoupling capacitor determines the loop area and hence the inductance. (b) Equivalent circuit. (c) Putting the decoupling capacitor near the chip and running power and return together reduces the loop area and inductance.

8.5 Cables and Connectors

- Connectors are the mechanical and electrical interface between cable and a circuit board.
- Shape or keying polarizes a connector so that it cannot be plugged in the wrong way.
- Reduce flexing of cables.
- Some guideline for connectors and cables:
    1) Pre-assign connector ground pins
    2) Distribute and intersperse grounds (return paths)
    3) Place clock next to a ground line
    4) Minimize I/O
    5) Use long rise and fall times to reduce high frequency harmonics
    6) Keep current to less than 1 amp per connector pin; otherwise use multiple pins or special pins or special pins with large current capacity.

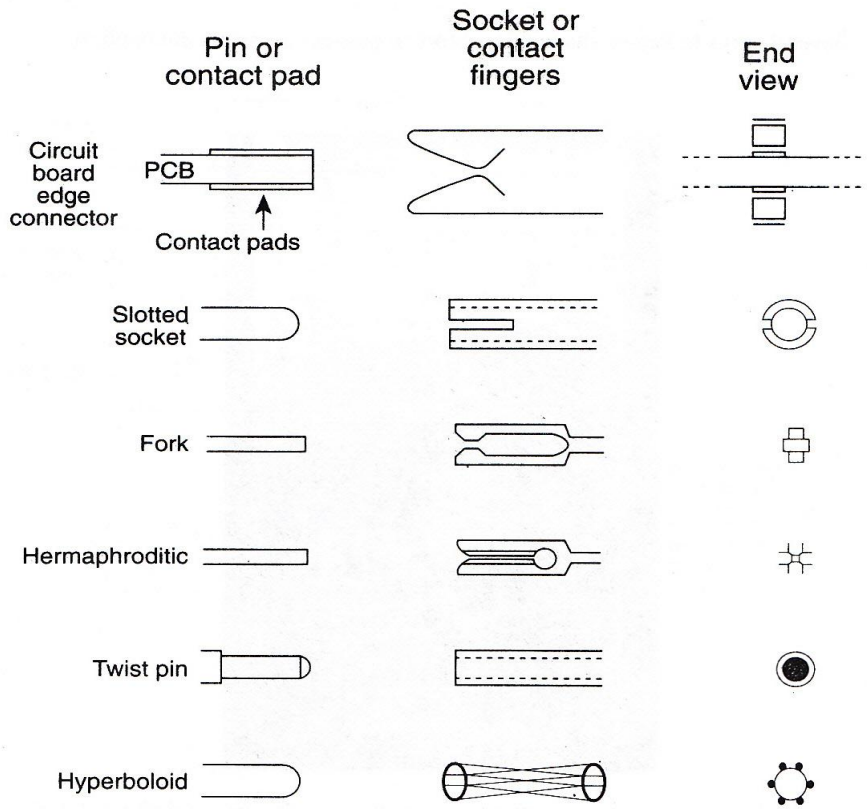


FIG. 8.17 Various configurations for connector pins, sockets, and contact fingers.

8.6 Testing and Maintenance

- Refer chapter 9